Please replace paragraph [0020] with the following rewritten paragraph:

-- An all digital PLL has one major drawback; the feedback signal and the reference typically will not be in phase, because the object of the PLL is to suppress certain signal artifacts. This lack of phase alignment directly translates to timing errors; the implicit sampling is discrete and therefor has rounding/trunking errors. This in itself may not seem too serious at a first glance, but it has a direct impact on the transfer function of the PLL, which is related to the transfer function of the phase detector. --

A2

Please replace paragraph [0027] with the following rewritten paragraph:

A3 -- Figure 1 is a functional block diagram of a digital controlled oscillator; --

Please replace paragraph [0028] with the following rewritten paragraph:

-- Figure 2 is a timing chart showing the effect of rejecting error components with high frequency; - -

A4

Please replace paragraph [0053] with the following rewritten paragraph:

A5 -- It may be impossible to detect any difference between very small, small, and normal error signals if they all fall in the region around the 0. This in turn makes it impossible to give any detail about the input signal by just looking at the output of the phase detector. It is precisely the details that are interesting if one would like to characterize for instance the noise behaviour of a telecomm line. The details may reveal effects such as noise typically from amplifiers, switches etc. These noise sources always will be small (otherwise the remaining information over the line is zero) and thus require a fine resolution for study. –

Please replace paragraph [0067] with the following rewritten paragraph:

A6 -- A decimator can be added if desired to derive a wanted error signal for a low frequency changing output. –

Please replace paragraph [0071] with the following rewritten paragraph:

-- Figure 10 shows a plurality of acquisition PLLs 1 connected through operational block 5 to output PLL 1. The acquisition PLLs 1 are connected through Muxes 6 to three inputs in 1, in 2, in 3, and crystal oscillator7. This embodiment allows the quality of the circuits to be tested. --